05.10.02

2841 #7

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Hui et al.

Serial No.: 09/916,197

Filed: July 27, 2001

For: METHOD FOR ENCAPSULATING INTERMEDIATE CONDUCTIVE ELEMENTS CONNECTING A SEMICONDUCTOR DIE TO A SUBSTRATE AND SEMICONDUCTOR DEVICES SO PACKAGED

Examiner: Unknown

Group Art Unit: 2841

Attorney Docket No.: 4712US (99-1054)

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EV 092592995 US

Date of Deposit with USPS: May 9, 2002

Person making Deposit: Blake Johnson

COMMUNICATION

Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed is a certified copy of priority document 200103014-7 filed May 21, 2001 for the above-referenced application.

Respectfully submitted,

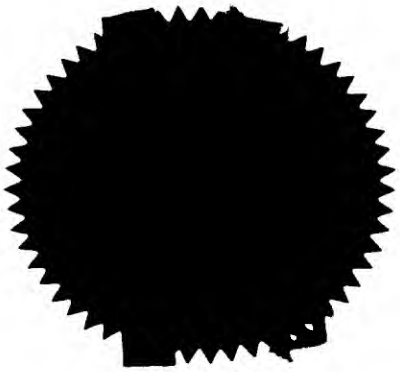
Brick G. Power
Registration No. 38,581
Attorney for Applicants
TRASK BRITT
P. O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: (801) 532-1922

Date: May 9, 2002
BGP/ps:djp
N:\2269\4712\Certified Priority Document Transmittal.wpd

REGISTRY OF PATENTS
SINGAPORE

This is to certify that the annexed is a true copy of the following Singapore patent application as filed in this Registry.

Date of Filing	:	21 MAY 2001
Application Number	:	200103014-7
Applicant(s)	:	MICRON TECHNOLOGY, INC.
Title of Invention	:	METHOD FOR ENCAPSUALTING INTERMEDIATE CONDUCTIVE ELEMENTS CONNECTING A SEMICONDUCTOR DIE TO A SUBSTRATE AND SEMICONDUCTOR DEVICES SO PACKAGED



Sharmaine Wu Shee Mei
Assistant Registrar
for REGISTRAR OF PATENTS
SINGAPORE

PATENTS FORM 1

Rule 19

SINGAPORE
PATENTS ACT
(CHAPTER 221)
PATENTS RULES

21 MAY 2001
200103014-7

The Registrar of Patents
Registry of Patents

REQUEST FOR THE GRANT OF A PATENT

THE GRANT OF A PATENT IS REQUESTED BY THE UNDERSIGNED ON THE BASIS OF THE PRESENT APPLICATION

I. Title of Invention	**METHOD FOR ENCAPSULATING INTERMEDIATE CONDUCTIVE ELEMENTS CONNECTING A SEMICONDUCTOR DIE TO A SUBSTRATE AND SEMICONDUCTOR DEVICES SO PACKAGED**	
II. Applicant(s) (*See note 2*)	***(a) Name***	**MICRON TECHNOLOGY, INC.**
	Body Description/ Residency	**A CORPORATION OF THE STATE OF DELAWARE, U.S.A.**
	Street Name & Number	**8000 SOUTH FEDERAL WAY** **BOISE, IDAHO 83707-0006**
	City	
	State	
	Country	**U.S.A.**
	(b) Name	
	Body Description/ Residency	
	Street Name & Number	
	City	
	State	
	Country	
	(c) Name	
	Body Description/ Residency	
	Street Name & Number	
	City	
	State	
	Country	

21 MAY 2001
200103014-7

III. Declaration of Priority (see note 3)	*Country/Country Designated*	**N.A**	*File no.*		**N.A.**
	Filing Date				
	Country/Country Designated		*File no.*		
	Filing Date				
	Country/Country Designated		*File no.*		
	Filing Date				

IV. Inventors (See note 4)		
(a) The applicant(s) is/are the sole/joint inventor(s).	[ ] *Yes* [X] *Yes*	[X] *No* [ ] *No*
(b) A statement on Patents Form 8 is/will be furnished.		
V. Name of Agent (if any) (See note 5)	**ARTHUR LOKE BERNARD RADA & LEE**	

VI. Address for Service (See note 6)	*Block/Hse No*		*Level No*	
	Unit No/PO Box	**#23-01**	*Postal Code*	**038989**
	Street Name	**9 TEMASEK BOULEVARD**		
	Building Name	**SUNTEC TOWER TWO**		

VII. Claiming an earlier filing date under section 20(3), 26(6) or 47(4). (See note 7)	*Application No*	**N.A.**
	Filing Date	

[Please tick in the relevant space provided]:

( ) Proceeding under rule 27(1)(*a*).
Date on which the earlier application was amended = _____
or
( ) Proceeding under rule 27(1)(*b*).

21 MAY 2001
200103014-7

VIII. Invention has been displayed at an International Exhibition (See note 8)	☐ *Yes* ☒ *No*
IX. Section 114 requirements (See note 9)	The invention relates to and/or used a micro-organism deposited for the purposes of disclosure in accordance with section 114 with a depository authority under the Budapest Treaty. ☐ *Yes* ☒ *No*

X. Check List

(To be filled in by applicant or agent)

A. The application contains the following number of sheet(s):-

1. Request	4	*sheets*
2. Description	12	*sheets*
3. Claim(s).	11	*sheets*
4. Drawing(s).	5	*sheets*
5. Abstract.	1	*sheets*

B. The application as filed is accompanied by:-

1. Priority document		
2. Translation of priority document		
3. Statement of Inventorship & right to grant		
4. International Exhibition Certificate		

XI. Signature(s)

(See note 10)

Applicant (a)		
Date	21 MAY 2001	[redacted]
Applicant (b)		
Date		[redacted]
Applicant (c)		
Date		[redacted]

21 MAY 2001
200103014-7

NOTES:

1. This form when completed, should be brought or sent to the Registry of Patents together with the prescribed fee and 3 copies of the description of the invention, and of any drawings.

2. Enter the name and address of each applicant in the spaces provided at paragraph II. Names of individuals should be indicated in full and the surname or family name should be underlined. The names of all partners in a firm must be given in full. The place of residence of each individual should also be furnished in the space provided. Bodies corporate should be designated by their corporate name and country of incorporation and, where appropriate, the state of incorporation within that country should be entered where provided. Where more than 3 applicants are to be named, the names and address of the fourth and any further applicants should be given on a separate sheet attached to this form together with the signature of each of these further applicants.

3. The declaration of priority at paragraph III should state the date of the previous filing, the country in which it was made, and indicate the file number, if available. Where the application relied upon in an International Application or a regional patent application e.g. European patent application, one of the countries designated in that application [being one falling under the Patents (Convention Countries) Order] should be identified and the name of that country should be entered in the space provided.

4. Where the applicant or applicants is/are the sole inventor or the joint inventors, paragraph IV should be completed by marking the 'YES' Box in the declaration (a) and the 'NO' Box in the alternative statement (b). Where this is not the case, the 'NO' Box in declaration (a) should be marked and a statement will be required to be filed on Patents Form 8.

5. If the applicant has appointed an agent to act on his behalf, the agent's name should be indicated in the spaces available at paragraph V.

6. An address for service in Singapore to which all documents may be sent must be stated at paragraph VI. It is recommended that a telephone number be provided if an agent is not appointed.

7. When an application is made by virtue of section 20(3), 26(6) or 47(4), the appropriate section should be identified at paragraph VII and the number of the earlier application or any patent granted thereon identified. Applicants proceeding under section 26(6) should identify which provision in rule 27 they are proceeding under. If the applicants are proceeding under rule 27(1)(*a*), they should also indicate the date on which the earlier application was amended.

8. Where the applicant wishes an earlier disclosure of the invention by him at an International Exhibition to be disregarded in accordance with section 14(4)(c), then the 'YES' Box at paragraph VIII should be marked. Otherwise the 'NO' Box should be marked.

9. Where in disclosing the invention the application refers to one or more micro-organisms deposited with a depository authority under the Budapest Treaty, then the 'YES' Box at paragraph IX should be marked. Otherwise the 'NO' Box should be marked.

10. Attention is drawn to rules 90 and 105 of the Patent Rules. Where there are more than 3 applicants, see also Note 2 above.

11. Applicants resident in Singapore are reminded that if the Registry of Patents considers that an application contains information the publication of which might be prejudicial to the defence of Singapore or the safety of the public, it may prohibit or restrict its publication or communication. Any person resident in Singapore and wishing to apply for patent protection in other countries must first obtain permission from the Singapore Registry of Patents unless they have already applied for a patent for the same invention in Singapore. In the latter case, no application should be made overseas until at least 2 months after the application has been filed in Singapore.

For Official Use

Application Filing Date: / /

Request received on : / /

Fee received on : / /

Amount :

*Cash/Cheque/Money Order No:

**Delete whichever is inapplicable*

METHOD FOR ENCAPSULATING INTERMEDIATE CONDUCTIVE ELEMENTS CONNECTING A SEMICONDUCTOR DIE TO A SUBSTRATE AND SEMICONDUCTOR DEVICES SO PACKAGED

BACKGROUND

Field of the Invention

The present invention relates generally to methods for packaging an assembly including a semiconductor die and a substrate element, such as an interposer or a carrier substrate and, more specifically, to a method for introducing an encapsulant material over intermediate conductive elements electronically connecting a semiconductor die and a substrate element. Particularly, the method of the present invention includes disposing tape between the semiconductor die and the substrate element, the intermediate conductive elements being located within a slot formed in the tape, and introducing encapsulant material into the slot.

Background of the Related Art

The dimensions of many different types of state of the art electronic devices are ever decreasing. To reduce the dimensions of electronic devices, the way in which the microprocessors, memory devices, other semiconductor devices, and other electronic componentry of these devices are packaged and assembled with circuit boards must become more compact.

One approach to reducing the sizes of assemblies of semiconductor devices and circuit boards has been to reduce the profiles of semiconductor devices and other electronic components upon carrier substrates (e.g., circuit boards) by reducing the distances the semiconductor devices or other electronic components protrude from the carrier substrates. Various types of packaging technologies have been developed to facilitate orientation of semiconductor devices upon carrier substrates in this manner.

"Flip-chip" technology, one example of which is termed controlled collapse chip connection (C-4) technology, is an example of a packaging and assembly technology that results in a semiconductor device being oriented substantially parallel to a carrier substrate, such as a circuit board. In flip-chip technology, the bond pads or contact pads of a semiconductor device are arranged in an array over a major surface of the

semiconductor device. Flip-chip techniques are applicable to both bare and packaged semiconductor devices. A packaged flip-chip type semiconductor device, which, when an array of discrete conductive elements is located over the major surface, is referred to in the art as a "ball grid array" (BGA) package, typically includes a semiconductor die and a substrate, which is typically termed an "interposer".

When the interposer of a ball grid array package is positioned adjacent the front surface of the semiconductor die thereof, the bond pads of the semiconductor die on one side of the interposer may be electrically connected to corresponding contact areas on a surface of the opposite side of the interposer by way of intermediate conductive elements, such as bond wires, that extend through one or more holes formed in the interposer. The contact areas communicate through conductive traces with corresponding contact pads bearing discrete conductive elements. In this type of flip-chip semiconductor device assembly, the contact pads are located on the same side of the interposer as the contact pads. This type of flip-chip assembly is positioned adjacent a carrier substrate by orienting the interposer with the contact pad-bearing side thereof facing the carrier substrate.

The contact pads of the interposer are disposed in an array that has a footprint that mirrors an arrangement of corresponding terminals formed on a carrier substrate. Each of the bond (on bare flip-chip semiconductor dice) or contact (on flip-chip packages) pads and its corresponding terminal as the contacts pads may be electrically connected to one another by way of a conductive structure in the form of a discrete conductive element, such as a solder ball, that also spaces the interposer some distance away from the carrier substrate. The space between the interposer and the carrier substrate may be left open or filled with a so-called dielectric "underfill" material that provides electrical insulation between the semiconductor device and the carrier substrate and enhances the mechanical connection between the two components.

In addition, the intermediate conductive elements that connect the bond pads of the semiconductor die to their corresponding contact areas on the substrate may be encapsulated by introducing material into the opening or openings of the interposer from above the contact pad-bearing side thereof. "Glob-top" type encapsulant materials, such as silicones or epoxies, are typically used for this purpose. Typically, glob-top encapsulant materials have a relatively high viscosity so that the material may be applied

to a substantially planar surface without being laterally confined over a particular area of that surface. In comparison with lower viscosity molding materials, such as transfer molding compounds, which are typically used with some structure to laterally confine the molding material over a specific region of an interposer, the height of the resulting glob-top-encapsulated structure may be greater at or near a centerline of the interposer opening than the encapsulant material thickness that would otherwise be required to properly encapsulate the wire bonds or other intermediate conductive elements that extend over regions of the surface of an interposer that are located adjacent a periphery of an opening formed therethrough. As a result, the overall height of a glop-top encapsulating structure may be undesirably high, proving an undesirably thick semiconductor device package.

Accordingly, there is a need for a method for encapsulating connetions between an interposer and semiconductor die of a semiconductor device assembly that facilitates leak-free introduction of encapsulant from the backside of the smiconductor die and a resulting semiconductor device assembly.

SUMMARY OF THE INVENTION

The present invention includes a semiconductor device assembly packaging method and semiconductor devices packaged in accordance with the method.

A packaging method incorporating teachings of the present invention includes assembling a semiconductor die with a substrate element, such as an interposer or a carrier substrate, by disposing a two-sided adhesive tape or other substantially planar member with adhesive on at least portions of both surfaces thereof between the active surface of the semiconductor die and the backside of the substrate element. Bond pads of the semiconductor die are exposed through a slot formed in the tape, as well as through an opening formed through the substrate element and aligned with the slot. At least one end and, preferably, both ends of the slot formed through the tape extend beyond an outer periphery of the semiconductor die. It is preferred, however, that neither end of the slot extends beyond an outer periphery of the substrate element with which the semiconductor die is assembled.

Wire bonds or other suitable intermediate conductive elements (e.g., tape-automated bonds (TABs) or thermocompression bonds) may be formed between the

bond pads of the semiconductor die and the corresponding contacts of the substrate element. Of course, these intermediate conductive elements extend through the slot of the tape and the opening of the substrate element.

A coverlay, such as a tape or other substantially planar member having a single side thereof coated with adhesive material, may be disposed over the exposed surface of the substrate element opposite the semiconductor die so as to cover the intermediate conductive elements extending through the substrate element. The coverlay preferably substantially seals the outer substrate element side of the opening formed by the slots of the substrate element and the tape. Thus, the intermediate conductive elements are substantially contained by interior lateral edges of the substrate element and the tape, as well as by the semiconductor die and the coverlay, the only exception being that one or both ends of the slot formed through the tape may be exposed beyond the outer periphery of the semiconductor die. The coverlay may also include one or more recessed areas that are configured to receive the intermediate conductive elements without contacting any portion thereof.

Next, liquid or gel-like encapsulant material is introduced from above, with the coverlay at the bottom of the assembly, into the slot formed through the tape and the aligned opening formed through the substrate element. The encapsulant material is preferably introduced into the slot through an end thereof that is exposed beyond an outer periphery of the semiconductor die. As encapsulant material fills the slot of the tape and the opening of the substrate element, air is displaced in the channel defined between the semiconductor die, the coverlay and the sides of the aligned tape slot and substrate element opening through another, opposite end of the slot, which is also exposed beyond an outer periphery of the semiconductor die.

Once the encapsulant material within the channel cures or otherwise becomes at least semisolid, the coverlay may be removed from the substrate element, or contact pads on the substrate element may be exposed through the coverlay and discrete conductive elements may be applied thereto or formed thereon. The packaged semiconductor device may then be tested and used, as known in the art.

Other features and advantages of the present invention will become apparent to those of skill in the art through consideration of the ensuing description, the accompanying drawings, and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings, which illustrate exemplary embodiments for carrying out the invention:

FIG. 1 is a perspective view of an assembly including a semiconductor die, a two-sided adhesive tape positioned on and secured to an active surface of the semiconductor die with bond pads of the semiconductor die being exposed through a slot in the tape, and a substrate element secured to an opposite side of the tape from the semiconductor die, the slot of the tape and the bond pads of the semiconductor die being exposed through an aligned opening in the substrate element;

FIG. 1A is an inverted perspective view of the assembly shown in FIG. 1;

FIG. 2 is a cross-section taken along line 2–2 of FIG. 1, illustrating the bond pads of the semiconductor die, the slot formed through the tape, and the aligned opening in the substrate element through which the bond pads of the semiconductor die are exposed;

FIG. 3 is a cross-sectional representation of the assembly shown in FIG. 2, depicting the placement of intermediate conductive elements between the bond pads of the semiconductor die and corresponding contact areas or contact pads on the exposed surface of the substrate element;

FIG. 4 is a cross-sectional representation of the assembly of FIG. 3, illustrating the positioning of a coverlay over at least a portion of an exposed surface of the substrate element to cover and at least partially contain the intermediate conductive elements that extend between the bond pads of the semiconductor die and their corresponding contact areas or pads of the substrate element;

FIG. 4A is a cross-sectional representation of the assembly in FIG. 3, illustrating the positioning of a variation of a coverlay, which includes a recessed area, over at least a portion of the exposed surface of the substrate element to cover and at least partially contain the intermediate conductive elements;

FIG. 4B is a cross-sectional representation of an assembly similar to that depicted in FIG. 3, but including a variation of the substrate element which includes a recessed area around the opening of the substrate element, and also including a coverlay over at least a portion of the exposed surface of the substrate element to cover and at least partially contain the intermediate conductive elements;

FIG. 5 is an inverted perspective view of the assembly of FIG. 4, schematically depicting the introduction of encapsulant material into the slot formed through the tape and the aligned opening through the substrate element from above with the backside of the semiconductor die facing upward;

FIG. 6 is a cross-section taken along line 6–6 of FIG. 5, showing the flow of encapsulant material into the slot formed through the tape and the aligned opening through the substrate element and around the intermediate conductive elements therein;

FIG. 7 is a perspective view of a package resulting from the process depicted in FIGs. 1-6 when the coverlay depicted in FIG. 4 is used;

FIG. 7A is a perspective view of a package resulting from the process depicted in FIGs. 1-6 when the coverlay depicted in FIG. 4A is used;

FIG. 7B is a perspective view of a package resulting from the process depicted in FIGs. 1-6 when the substrate element and coverlay depicted in FIG. 4B are used;

FIG. 8A is a perspective assembly view of a substrate element strip with tape secured to a backside thereof and of semiconductor dice to be assembled with the substrate element strip;

FIG. 8B is a perspective view of an assembly including each of the elements shown in FIG. 8A; and

FIG. 8C is a perspective view of the assembly of FIG. 8B, depicting discrete conductive elements being secured to contact pads of the substrate element.

DETAILED DESCRIPTION OF THE INVENTION

Referring to FIGs. 1, 1A, and 2, an assembly 1 is illustrated that includes a semiconductor die 10, a substrate element 30, and a dielectric tape 20 positioned between semiconductor die 10 and substrate element 30.

Semiconductor die 10 includes an active surface 11 and an opposite backside 12. Bond pads 14, which facilitate the communication of electrical signals to and from the various integrated circuits of semiconductor die 10, are carried upon active surface 11. While FIG. 1 illustrates bond pads 14 as being arranged substantially linearly along the center of active surface 11, in a pattern that is typically used to assemble a semiconductor die 10 with a leads-over-chip (LOC) type lead frame, methods

incorporating teachings of the present invention are equally applicable to packaging semiconductor dice with different bond pad arrangements.

Tape 20 is a substantially planar member with two surfaces 21 and 22 that are preferably at least partially coated with adhesive material. Tape 20 also includes a slot 24 formed therethrough, which includes two closed ends. Slot 24 is located such that bond pads 14 of semiconductor die 10 are exposed therethrough when tape 20 is properly aligned over and secured to active surface 11 of semiconductor die 10.

The material from which tape 20 is formed preferably exhibits a similar coefficient of thermal expansion (CTE) to that of the material of semiconductor die 10. For example, a polyimide tape 20 would be useful with a semiconductor die 10 formed on a silicon substrate element. When semiconductor die 10 and tape 20 have substantially similar, or "matched", coefficients of thermal expansion, the likelihood that these elements of a package will be mechanically stressed during thermal cycling occurring in testing or operation of semiconductor die 10 is reduced.

As shown, substrate element 30 is an interposer with opposed surfaces 31 and 32. The dimensions of surfaces 31 and 32 of substrate element 30 may be substantially the same as the corresponding dimensions of surfaces 21 and 22of tape 20. An opening 34 formed through substrate element 30 aligns with bond pads 14 of semiconductor die 10 through slot 24 such that bond pads 14 are exposed through opening 34 when substrate element 30 is properly positioned over active surface 11 of semiconductor die 10. Preferably, opening 34 is substantially the same size and shape as slot 24 of tape 20 and is aligned therewith upon securing tape 20 to a surface 31 of substrate element 30.

Substrate element 30 also includes contact areas 36 on surface 31 thereof. Each contact area 36 corresponds to a bond pad 14 of semiconductor die 10. In addition, surface 31 of the illustrated substrate element 30 carries contact pads 38, each of which corresponds to a contact area 36 and communicates therewith by way of a conductive element 37 that extends between contact pad 38 and contact area 36.

The material from which substrate element 30 is formed preferably has a coefficient of thermal expansion that is similar to or substantially the same as those of the materials of tape 20 and semiconductor die 10. For example, a substrate element 30 formed from silicon would have a similar coefficient of thermal expansion to those of a

polyimide tape 20 and a silicon semiconductor die 10. Alternatively, other materials that may be used to fabricate flexible or rigid substrate elements, such as ceramics, FR-4 resin, or polyimide, may be used to form substrate element 30.

While the drawings depict substrate element 30 as being an interposer, the method of the present invention may also be used to package assemblies with other types of substrate elements, including, without limitation, other carrier substrate elements.

In forming assembly 1, tape 20 may be positioned relative to and secured to both active surface 11 of semiconductor die 10 and surface 32 of substrate element 30. When semiconductor die 10, tape 20, and substrate element 30 are properly positioned relative to one another, bond pads 14 of semiconductor die 14 are exposed through both slot 24 of tape 20 and aligned opening 34 of substrate element 30.

As shown in FIG. 1A, ends 25 and 26 of slot 24 formed through tape 20 and corresponding ends of opening 34 may extend beyond an outer periphery 15 of semiconductor die 10. Preferably, however, neither end 25, 26 of slot 24 extends beyond an outer periphery 35 of substrate element 30.

Once semiconductor die 10, tape 20, and substrate element 30 have been properly positioned relative to one another and secured to one another to form assembly 1, each bond pad 14 of semiconductor die 10 may be electrically connected to its corresponding contact area 36 of substrate element 30. As shown in FIG. 3, this may be done by placing or forming an intermediate conductive element 40, such as the illustrated wire bond or a tape-automated bond (i.e., flex circuit) or thermocompression bond, between each bond pad 14 and its corresponding contact area 36, through slot 24 of tape 20 and opening 34 of substrate element 30, and by bonding respective ends of intermediate conductive element 40 to bond pad 14 and to contact area 36, as known in the art.

Since slot 24 and opening 34 extend beyond outer periphery 15 of semiconductor die 10, as shown in FIG. 1A, apparatus that form or position intermediate conductive elements 40, such as a wire bonding capillary, may better access bond pads 14 located at or near outer periphery 15.

Turning now to FIG. 4, a coverlay 42, which may comprise tape or another substantially planar member, one side of which is coated with adhesive material, is

positioned on surface 31 of substrate element 30. While coverlay 42 may cover substantially the entire surface 31, coverlay need only substantially cover opening 34 and intermediate conductive elements 40 that extend through opening 34. Coverlay 42 may be aligned with surface 31 by known processes and secured thereto, as known in the art. The adhesive material of coverlay 42 preferably facilitates the ready removal of coverlay 42 from surface 31 once coverlay 42 is no longer needed. By way of example, a pressure sensitive adhesive that will withstand the conditions of subsequent processes may be used on coverlay 42. Coverlay 42 preferably has sufficient flexibility to conform to any irregularities or nonplanarities of surface 31 of substrate element 30, such as the portions of intermediate conductive elements 40 that extend over surface 31 and contact areas 36 located on surface 31.

Once coverlay 42 has been secured to surface 31 of substrate element 30 and over opening 34 thereof, intermediate conductive elements 40 are at least partially laterally contained within a receptacle formed by coverlay 42, the peripheral edges of opening 34, and the peripheral edges of slot 24 formed through tape 20. At the side of opening 34 opposite tape 20, intermediate conductive elements 40 are contained by coverlay 42. In addition, with the exception of the exposed ends 25, 26 (FIG. 1A) of slot 24 that are located outside the periphery 15 of semiconductor device 10, intermediate conductive elements 40 are also partially contained by semiconductor device 10.

As depicted in FIG. 4, coverlay 42 includes a single, substantially planar layer of material. Alternatively, as shown in FIG. 4A, a variation of coverlay 42′ includes two layers 42a′ and 42b′, one layer 42a′ of which is substantially continuous, while the other layer 42b′ includes an aperture 43′ therethrough. When layers 42a′ and 42b′ are secured to one another, aperture 43′ forms a recess 44′ within a surface of coverlay 42′. Aperture 43′ and recess 44′ formed thereby are located to receive the portions of intermediate conductive elements 40 that extend over surface 31 of substrate element 30 upon placement of coverlay 42′ on surface 31. Preferably, when coverlay 42′ is secured to surface 31, coverlay 42′ does not contact any portion of intermediate conductive elements 40, thereby subsequently facilitating the substantially complete encapsulation of intermediate conductive elements 40.

Alternative means by which intermediate conductive elements 40 may be substantially contained and subsequently encapsulated are shown in FIG. 4B, which illustrates a variation of a substrate element 30″ that may be used in methods and semiconductor device packages incorporating teachings of the present invention. A surface 31″ of substrate element 30″ may include a recessed area 33″ which surrounds opening 34″. Recessed area 33″, within which conductive areas 36″ are located, is configured to receive the portions of intermediate conductive elements 40 that extend over surface 31″. Accordingly, a substantially planar coverlay 42, such as that described in reference to FIG. 4, may be secured to surface 31″ of substrate element 30″ without substantially contacting intermediate conductive elements 40.

FIGs. 5 and 6 show assembly 1 in an inverted orientation, with backside 12 of semiconductor die 10 and the exposed ends 25, 26 of slot 24 formed through tape 20 facing upward. Using an encapsulant dispenser needle 50 of a type known in the art, a suitable, known type of dielectric encapsulant material 52 may be introduced into slot 24 of tape and opening 34 of substrate element 30 through an exposed end 25 of slot 24. As encapsulant material is being introduced into slot 24, air within slot 24 is displaced through the other end 26 thereof. In addition to containing encapsulant material 52 within slot 24 and opening 34, coverlay 42 also laterally confines encapsulant material 52 over surface 31 of substrate element 30. Preferably, when slot 24 and opening 34 are substantially filled with encapsulant material 52, encapsulant material 52 substantially encapsulates intermediate conductive elements 40.

Once slot 24 and opening 34 are substantially completely filled with encapsulant material 52, encapsulant material 52 may be permitted to harden, if a thermoplastic resin, or known processes may be employed to cure or set other types of encapsulant materials 52 (e.g., by application of heat and/or pressure to thermoset resins, by exposure of photoimageable polymer encapsulant materials to an appropriate wavelength of radiation, or by use of an appropriate catalyst for other types of materials). Together, encapsulant material 52 and tape 20 substantially encapsulate active surface 11 of semiconductor device 10 and fill the gap between active surface 11 and surface 32 of substrate element 30.

Once encapsulant material 52 has hardened, all or a portion of coverlay 42, 42′ may be removed from substrate element 30, 30″ so as to expose at least contact

pads 38, 38′ thereof, as depicted in FIGs. 7, 7A, and 7B, and form an operable semiconductor device package 2, 2′, 2″.

An alternative method for packaging semiconductor dice 10 in accordance with teachings of the present invention, which involves the use of substrate element strips 3‴, each of which includes a plurality of connected substrate elements 30‴ formed thereon, is shown in FIGs. 8A and 8B.

As shown in FIG. 8A, each substrate element 30‴ of substrate element strip 3‴ includes an elongate opening 34‴ formed therethrough, as well as contact areas 36‴ positioned on a surface 32‴ of substrate element 30‴, proximate its opening 34‴ and contact pads 38‴ corresponding to and in communication with contact areas 36‴.

An elongate tape 20‴, which includes a plurality of slots 24‴ formed therethrough, each slot 24‴ corresponding to an opening of a substrate element 30‴ of substrate element strip 3‴, may be positioned adjacent and secured to a backside 31‴ of substrate element strip 3‴.

A semiconductor die 10 may be aligned with each substrate element 30‴ formed on substrate element strip 3‴, as shown in FIG. 8A, and secured to substrate element 30‴ by way of tape 20‴, as illustrated in FIG. 8B. When semiconductor dice 10 are properly positioned, upon securing semiconductor dice 10 to tape 20‴ and, thus, to substrate element strip 3‴, bond pads 14 on each semiconductor die 10 are exposed through their corresponding slot 24‴ of tape 20‴, as well as through their corresponding opening 34‴ of the corresponding substrate element 30‴.

In addition, as depicted in FIG. 8C, discrete conductive elements 2 may be formed on or secured to terminals 38‴ on surface 32‴ of each substrate element 30‴ to facilitate connection of each substrate element 30‴ to a higher level substrate, such as a circuit board, or to another semiconductor device, as known in the art. Discrete conductive elements 2 may comprise, for example, balls, bumps, pillars, columns, or other structures formed from one or more metals (e.g., solder, gold, etc.), conductive epoxies, conductor-filled epoxies, or z-axis conductive elastomers.

Once each semiconductor die 10 and its corresponding substrate element 30‴ have been electrically connected to each other and packaged, such as by the processes disclosed herein in reference to FIGs. 3-6, adjacent packages may be separated severed

from one another by known techniques, such as by use of a wafer saw or otherwise, as known in the art.

In the illustrated embodiments of the inventive semiconductor device package, tape 20 comprises the majority of material between semiconductor die 10 and substrate element 30, while encapsulant material 52 covers a relatively small portion of active surface 11 of semiconductor die 10. If, as is preferred, the coefficient of thermal expansion of tape 20 is substantially the same as or similar enough to the coefficient of thermal expansion of semiconductor die 10, the thermally induced mechanical stresses (i.e., by adjacent, thermally mismatch layers or structures) that will be applied to package during operation of semiconductor die 10 will be minimized. If substrate element 30 is also formed from silicon or another material having substantially the same or a similar enough coefficient of thermal expansion to that of semiconductor die 10, thermally induced mechanical stresses on package 2, 2′, 2″ will be further minimized.

Although the foregoing description contains many specifics, these should not be construed as limiting the scope of the present invention, but merely as providing illustrations of some exemplary embodiments. Similarly, other embodiments of the invention may be devised which do not depart from the spirit or scope of the present invention. Features from different embodiments may be employed in combination. The scope of the invention is, therefore, indicated and limited only by the appended claims and their legal equivalents, rather than by the foregoing description. All additions, deletions, and modifications to the invention, as disclosed herein, which fall within the meaning and scope of the claims are to be embraced thereby.

CLAIMS

What is claimed is:

1. A semiconductor device package, comprising:

a semiconductor die with a plurality of bond pads arranged on an active surface thereof;

a tape positioned over said active surface, said tape including at least one slot formed therethrough, each of said plurality of bond pads being exposed through said slot, at least one end of said slot extending beyond an outer periphery of said semiconductor die;

a substrate element positioned over said tape opposite said semiconductor die, said substrate element including a plurality of contact areas, each contact area of said plurality corresponding to a bond pad of said plurality of bond pads and electrically connected thereto by way of an intermediate conductive element that extends through at least one opening formed through said substrate element and aligned with said slot of said tape, said substrate element further including a contact pad in communication with each contact area of said plurality of contact areas by way of a substantially laterally extending conductive trace; and

a quantity of encapsulant material substantially filling a volume defined by said slot of said tape and said at least one opening of said substrate element.

2. The semiconductor device package of claim 1, wherein said plurality of bond pads is arranged substantially lineraly along a central region of said active surface of said semiconductor die.

3. The semiconductor device package of claim 1, wherein said tape is formed from a material having a coefficient of thermal expansion similar to a coefficient of thermal expansion of a material of said semiconductor die.

4. The semiconductor device package of claim 3, wherein said substrate element has a coefficient of thermal expansion similar to said coefficient of thermal expansion of said material of said semiconductor die.

5. The semiconductor device package of claim 1, wherein both ends of said slot formed through said tape extend beyond said outer periphery of said semiconductor die.

6. The semiconductor device package of claim 1, wherein said tape is adhesively secured to said active surface of said semiconductor die and to said substrate element.

7. The semiconductor device package of claim 1, wherein said substrate element comprises at least one of an interposer and a carrier substrate.

8. The semiconductor device package of claim 1, wherein said substrate element comprises silicon.

9. The semiconductor device package of claim 1, wherein said quantity of encapsulant material substantially encapsulates each intermediate conductive element.

10. The semiconductor device package of claim 9, wherein said quantity of encapsulant material protrudes above a major plane of an exposed surface of said substrate element opposite said semiconductor die.

11. The semiconductor device package of claim 1, wherein said substrate element includes a recessed area adjacent said at least one opening, each contact area of said plurality of contact areas being located within said recessed area.

12. The semiconductor device package of claim 11, wherein said encapsulant material substantially fills said recessed area.

13. The semiconductor device package of claim 12, wherein said quantity of encapsulant material substantially encapsulates each said intermediate conductive element.

14. The semiconductor device package of claim 12, wherein said quantity of encapsulant material does not extend substantially beyond a major plane of an exposed surface of said substrate element.

15. The semiconductor device package of claim 1, further comprising a coverlay positioned on a surface of said substrate element opposite said tape, said coverlay substantially covering at least said at least one opening through said substrate element.

16. The semiconductor device package of claim 15, wherein said coverlay comprises a recessed area within which each intermediate conductive element is contained.

17. The semiconductor device package of claim 15, wherein said coverlay is secured to said substrate element with an adhesive material.

18. The semiconductor device package of claim 17, wherein said adhesive material comprises a pressure sensitive adhesive material.

19. The semiconductor device package of claim 15, wherein contact pads of said substrate element are exposed through or beyond said coverlay.

20. The semiconductor device package of claim 1, further comprising discrete conductive elements protruding from at least some of said contact pads.

21. A semiconductor device assembly, comprising:

a semiconductor die with at least one bond pad on an active surface thereof;

a tape secured to said active surface, said tape including a slot formed therethrough with said at least one bond pad being exposed through said slot, at least one end of said slot extending beyond an outer periphery of said semiconductor die; and

a substrate element positioned over said semiconductor die opposite said tape from said semiconductor die, said substrate element including at least one opening formed therethrough through which said at least one bond pad is exposed.

22. The assembly of claim 21, wherein said semiconductor die includes a plurality of bond pads arranged substantially linearly along a central region of said active surface.

23. The assembly of claim 21, wherein said tape has a similar coefficient of thermal expansion to a coefficient of thermal expansion of said substrate element.

24. The assembly of claim 23, wherein said substrate element has a similar coefficient of thermal expansion to said coefficient of thermal expansion of said semiconductor die.

25. The assembly of claim 21, wherein two ends of said slot extend beyond said outer periphery of said semiconductor die.

26. The assembly of claim 21, wherein said at least one end of said slot receives encapsulant material.

27. The assembly of claim 26, wherein one of said two ends of said slot is positioned so as to facilitate the displacement of air from said slot while an encapsulant material is being introduced at least into a volume defined by said slot from the other of said two ends.

28. The assembly of claim 21, wherein said substrate element comprises at least one of an interposer, and a carrier substrate.

29. The assembly of claim 21, wherein said substrate element includes a recessed area formed adjacent said at least one opening in a surface of said substrate element located opposite said tape.

30. The assembly of claim 29, wherein said substrate element includes at least one contact area corresponding to said at least one bond pad of said semiconductor die.

31. The assembly of claim 30, wherein said at least one contact area is located within said recessed area.

32. The assembly of claim 31, wherein said recessed area receives a portion of an intermediate conductive element that extends between said at least one bond pad and said at least one contact area.

33. The assembly of claim 21, wherein said substrate element includes at least one contact area that corresponds to said at least one bond pad of said semiconductor die and at least one contact pad in electrical communication with said at least one contact area.

34. The assembly of claim 33, further comprising at least one intermediate conductive element electrically connecting said at least one bond pad to said at least one conductive area.

35. The assembly of claim 34, wherein said at least one intermediate conductive element extends through said slot of said tape and said at least one opening of said substrate element.

36. The assembly of claim 21, further comprising a coverlay disposed on a surface of said substrate element opposite another surface thereof positioned adjacent said tape, said coverlay positioned over said at least one opening formed through said substrate element.

37. The assembly of claim 36, wherein said coverlay includes a recessed area configured to communicate with said at least one opening.

38. The assembly of claim 37, wherein said recessed area is configured to receive a portion of at least one intermediate conductive element electrically connecting said at least one bond pad of said semiconductor die to a contact area on a surface of said substrate element adjacent said at least one opening formed therethrough.

39. The assembly of claim 36, wherein said coverlay, said at least one opening formed through said substrate element, said slot formed through said tape, and said semiconductor die together form a receptacle.

40. The assembly of claim 39, wherein said receptacle at least partially contains a quantity of encapsulant material.

41. A method for packaging at least an active surface of a semiconductor die, comprising:

positioning a tape over the active surface so that at least one bond pad on the active surface is exposed through a slot formed through said tape and at least one end of said slot extends beyond an outer periphery of the semiconductor die;

positioning a substrate element over said tape so that said at least one bond pad is exposed through at least one opening formed through said substrate element and aligned with said slot, said substrate element including at least one conductive area corresponding to said at least one bond pad;

electrically connecting said at least one bond pad to said at least one conductive area;

positioning a coverlay on an exposed surface of said substrate element to substantially cover said at least one opening formed through said substrate element; and

introducing encapsulant material through said at least one end into a receptacle formed by said coverlay, said at least one opening, said slot, and said semiconductor die from a location opposite the semiconductor die from said tape.

42. The method of claim 41, wherein said positioning said tape comprises positioning over the semiconductor die a tape having a similar coefficient of thermal expansion to a coefficient of thermal expansion of the semiconductor die.

43. The method of claim 42, wherein said positioning said substrate element comprises positioning over said tape a substrate element having a similar coefficient of thermal expansion to said coefficient of thermal expansion of the semiconductor die.

44. The method of claim 43, wherein said positioning said substrate element comprises positioning a substrate element comprising silicon over said tape.

45. The method of claim 41, wherein said positioning said tape comprises orienting said slot with another end thereof extending laterally beyond said outer periphery of the semiconductor die.

46. The method of claim 41, further including securing said tape to the active surface of the semiconductor die.

47. The method of claim 46, wherein said securing comprises adhering said tape to the active surface.

48. The method of claim 41, wherein said positioning said substrate element comprises positioning at least one of an interposer and a carrier substrate over said tape.

49. The method of claim 41, wherein said positioning said substrate element comprises positioning over said tape a substrate element comprising a recessed area adjacent said at least one opening and including therein said at least one contact area.

50. The method of claim 49, wherein said introducing comprises introducing a portion of said quantity of encapsulant material into said recessed area.

51. The method of claim 41, wherein said electrically connecting comprises connecting at least one intermediate conductive element between said at least one bond pad and said at least one contact area.

52. The method of claim 51, wherein said connecting said at least one intermediate conductive element comprises wire bonding.

53. The method of claim 51, wherein said connecting said at least one intermediate conductive element comprises extending said at least one intermediate conductive element through said slot formed through said tape and said at least one opening formed through said substrate element.

54. The method of claim 41, wherein said positioning said coverlay comprises positioning over said substrate element a coverlay including a recessed area alignable over said at least one opening and over intermediate conductive elements extending through said at least one opening.

55. The method of claim 41, further including securing said substrate element to said tape.

56. The method of claim 55, wherein said securing comprises adhesively securing said substrate element to said tape.

57. The method of claim 41, further including securing said coverlay to said substrate element.

58. The method of claim 57, wherein said securing comprises securing said coverlay to said substrate element with a pressure sensitive adhesive.

59. The method of claim 58, wherein said securing comprises removably securing said coverlay to said substrate element.

60. The method of claim 41, wherein said introducing comprises substantially filling said slot formed through said tape and said at least one opening formed through said substrate element with said quantity of encapsulant material.

61. The method of claim 41, wherein said introducing comprises substantially encapsulating at least one intermediate conductive element electrically connecting said at least one bond pad to said at least one contact area.

62. The method of claim 41, wherein said positioning said coverlay comprises forming a receptacle, including said slot and said at least one opening, within which said at least one bond pad is located.

63. A method for preparing a semiconductor die for packaging, comprising:

positioning a tape over at least an active surface of the semiconductor die, said tape including a slot through which at least one bond pad on the active surface of the semiconductor die is exposed, at least a portion of said slot extending laterally beyond an outer periphery of the semiconductor die;

positioning a substrate element over said tape with at least one opening formed through said substrate element being located at least partially over said slot; and

positioning a coverlay over said substrate element to substantially seal said at least one opening, said coverlay and lateral edges of said at least one opening and said slot forming a receptacle.

64. The method of claim 63, further comprising electrically connecting said at least one bond pad to at least one conductive area located on a surface of said substrate element opposite said tape, proximate said at least one opening.

65. The method of claim 64, wherein said electrically connecting comprises connecting at least one intermediate conductive element between said at least one bond pad and said at least one contact area.

66. The method of claim 65, wherein said connecting said at least one intermediate conductive element comprises positioning said at least one intermediate conductive element at least partially within said slot and said at least one opening.

67. The method of claim 63, wherein said positioning said tape comprises positioning a tape having a coefficient of thermal expansion similar to a coefficient of thermal expansion of the semiconductor die.

68. The method of claim 67, wherein said positioning said substrate element comprises positioning over said tape a substrate element having a coefficient of thermal expansion similar to said coefficient of thermal expansion of the semiconductor die.

69. The method of claim 63, wherein said positioning said tape comprises positioning said tape with at least two regions of said slot extending laterally beyond said outer periphery of the semiconductor die.

70. The method of claim 63, further comprising securing said tape to the active surface of the semiconductor die.

71. The method of claim 70, wherein said securing comprises adhesively securing said tape to the active surface of the semiconductor die.

72. The method of claim 63, wherein said positioning said substrate element comprises positioning over said tape a substrate element including a recessed area adjacent at least a portion of an edge of said at least one opening, said at least one contact area being located within said recessed area.

73. The method of claim 63 wherein said positioning said substrate element comprises positioning over said tape a substrate element comprising at least one of an interposer and a carrier substrate.

74. The method of claim 63 further comprising securing said substrate element to said tape.

75. The method of claim 74 wherein said securing comprises adhesively securing said substrate element to said tape.

76. The method of claim 63 wherein said positioning said coverlay comprises positioning over said substrate element a coverlay comprising a recess formed therein, said recess being positioned so as to communicate with said at least one opening formed through said substrate element when said positioning is effected.

77. The method of claim 63 further comprising securing said coverlay to said substrate element.

78. The method of claim 77 wherein said securing comprises adhesively securing said coverlay to said substrate element.

79. The method of claim 77, wherein said securing comprises removably securing said coverlay to said substrate element.

METHOD FOR ENCAPSULATING INTERMEDIATE CONDUCTIVE ELEMENTS CONNECTING A SEMICONDUCTOR DIE TO A SUBSTRATE AND SEMICONDUCTOR DEVICES SO PACKAGED

ABSTRACT

A method for packaging semiconductor device assemblies. An assembly is formed which includes a semiconductor die, a tape positioned over the active surface of the die, and a substrate element positioned on an opposite side of the tape from the die. Bond pads of the die are exposed through a slot formed through the tape and an aligned an opening formed through the substrate element facilitate the extension of intermediate conductive elements from the bond pads and through the slot and opening, to corresponding contact areas on the substrate element. One or both ends of the slot extend beyond an outer periphery of the die to facilitate introduction of an encapsulant material into a channel or receptacles defined by the slot, opening, and active surface of the semiconductor die. Prior to encapsulation, the side of the opening of the substrate element is sealed opposite the tape with a coverlay to contain the encapsulant material within the channel or receptacle. Assemblies and packages formed by the method are also disclosed.

[Figure 1]

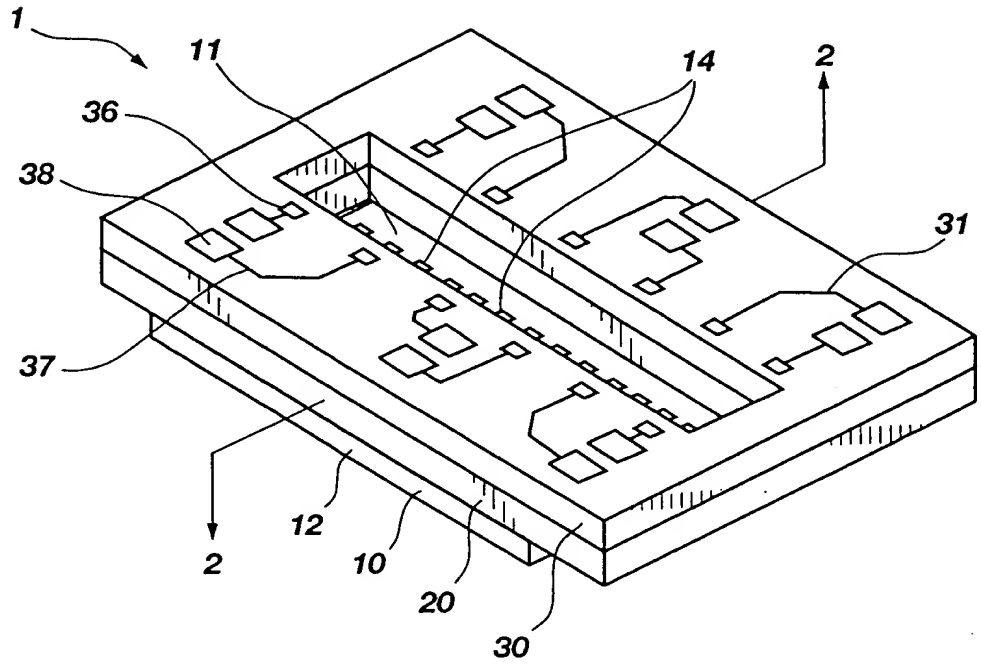


Fig. 1

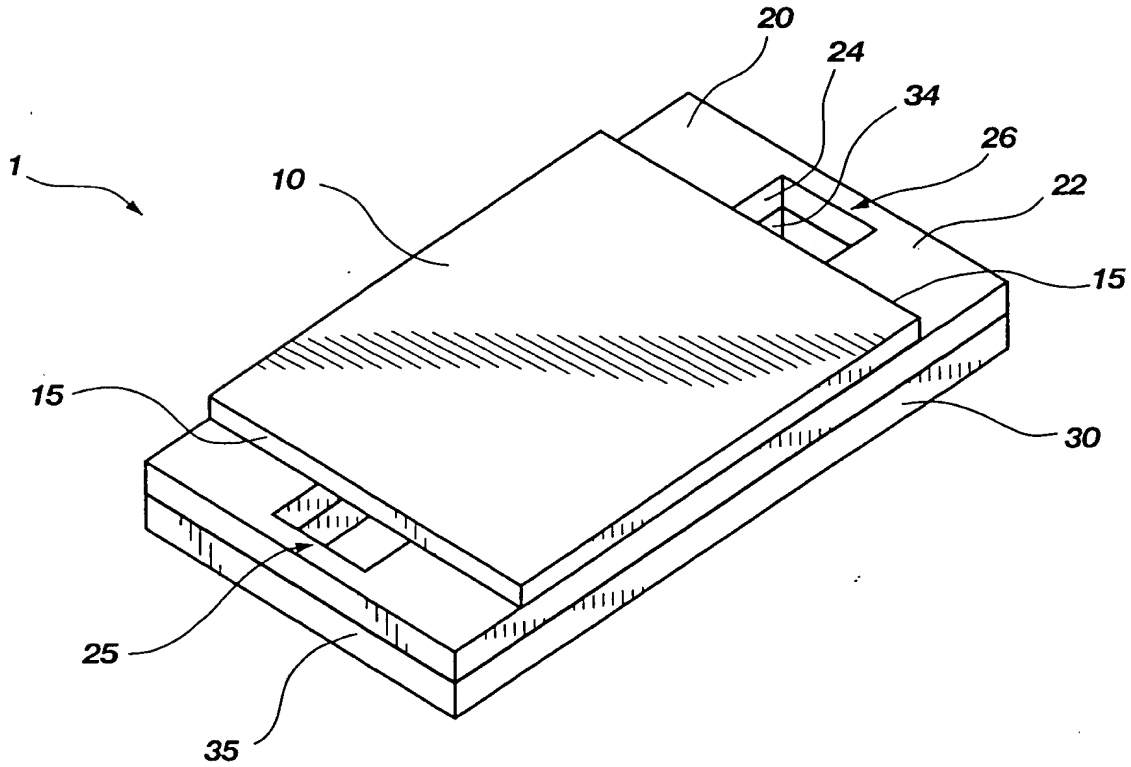


Fig. 1A

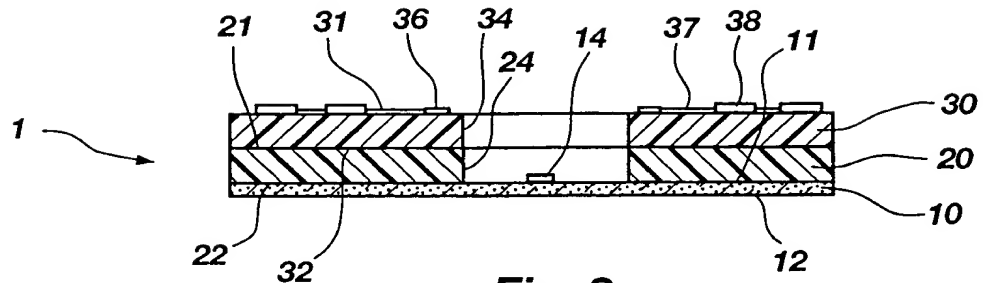


Fig. 2

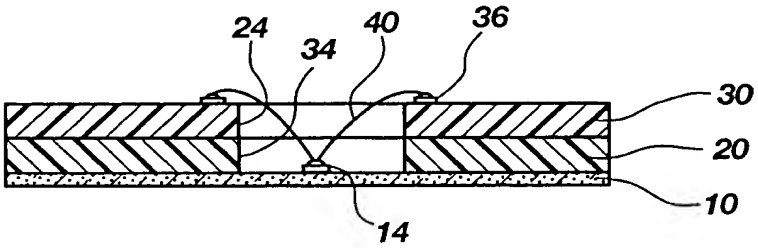


Fig. 3

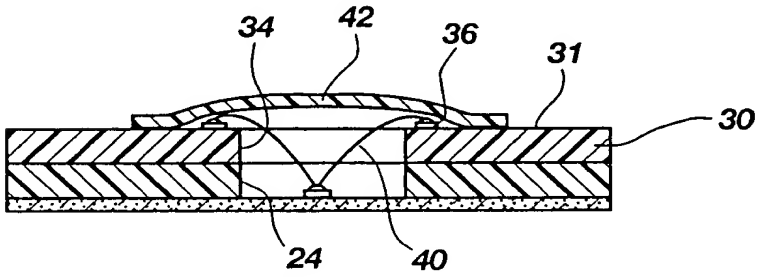


Fig. 4

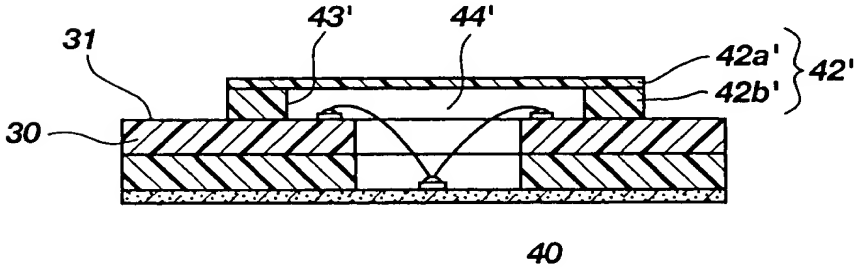


Fig. 4A

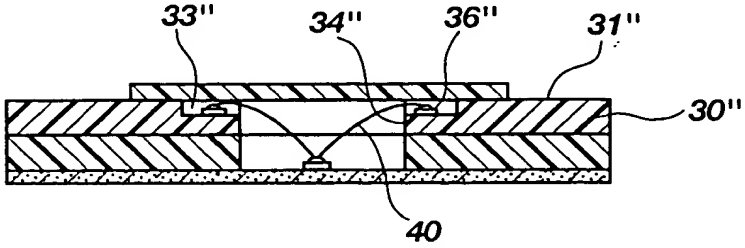


Fig. 4B

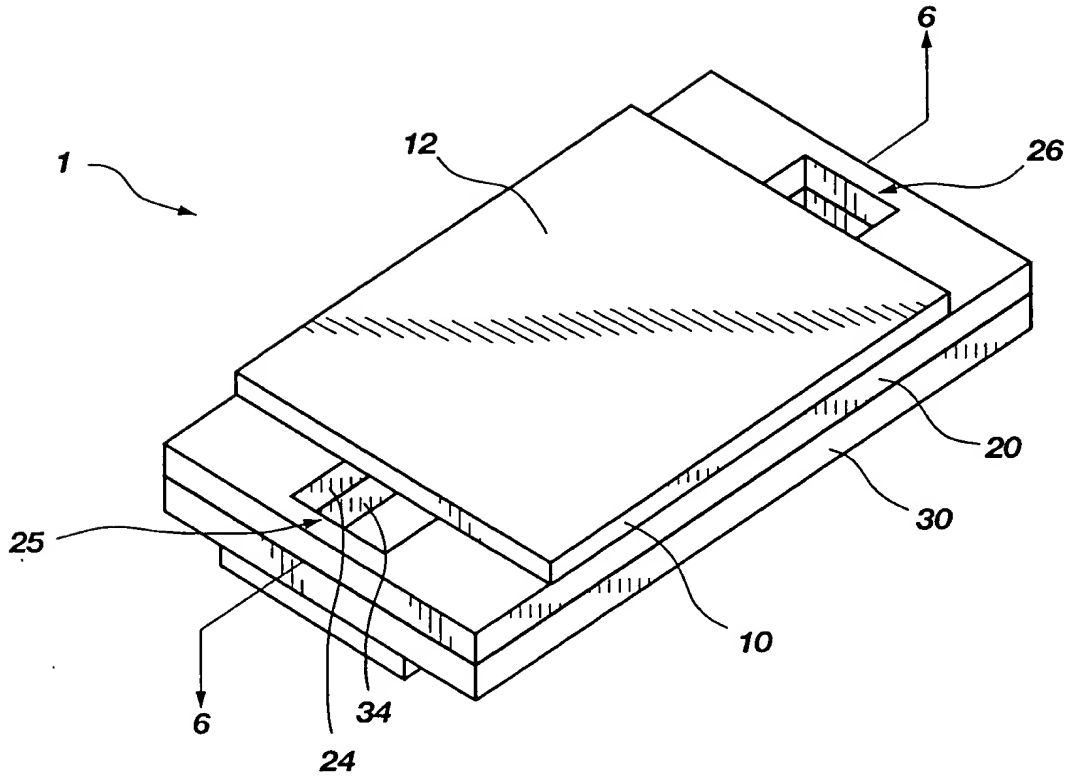


Fig. 5

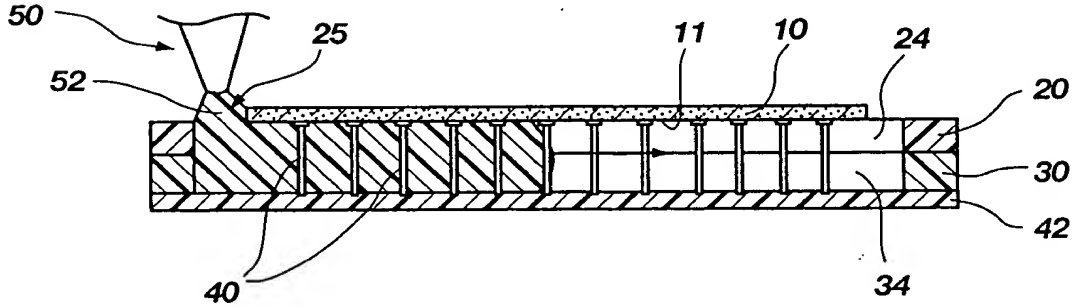


Fig. 6

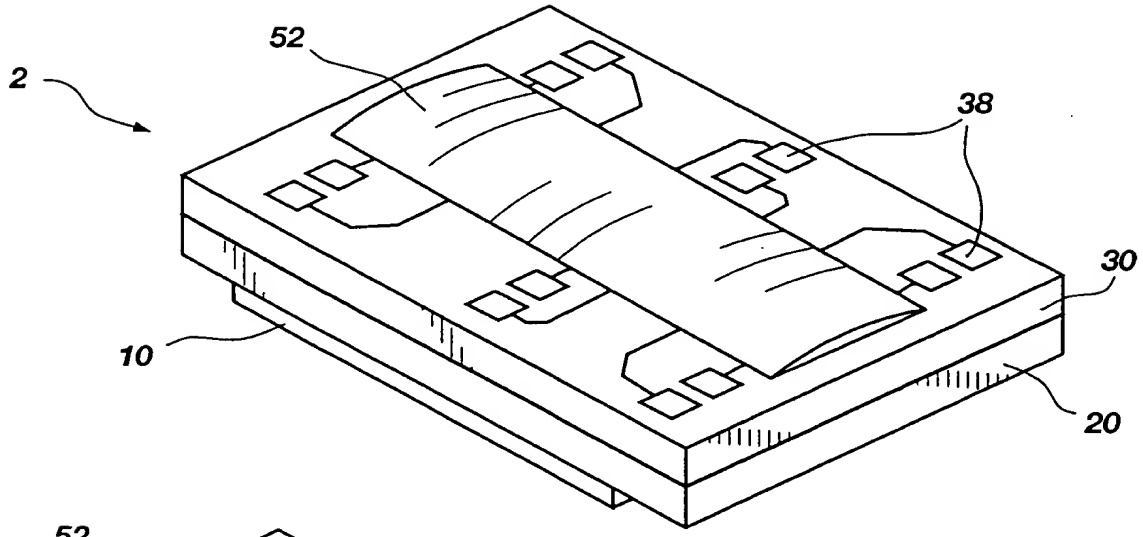


Fig. 7

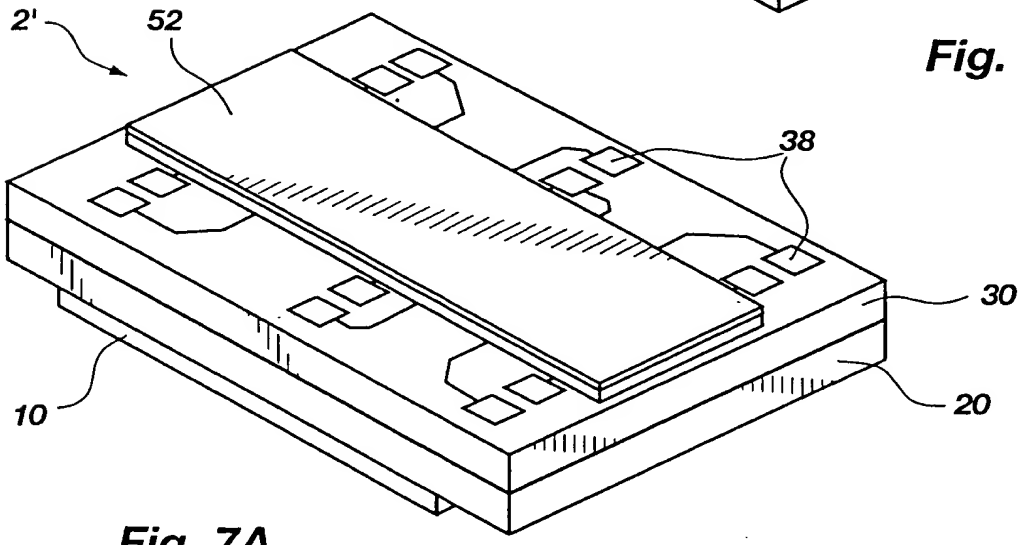


Fig. 7A

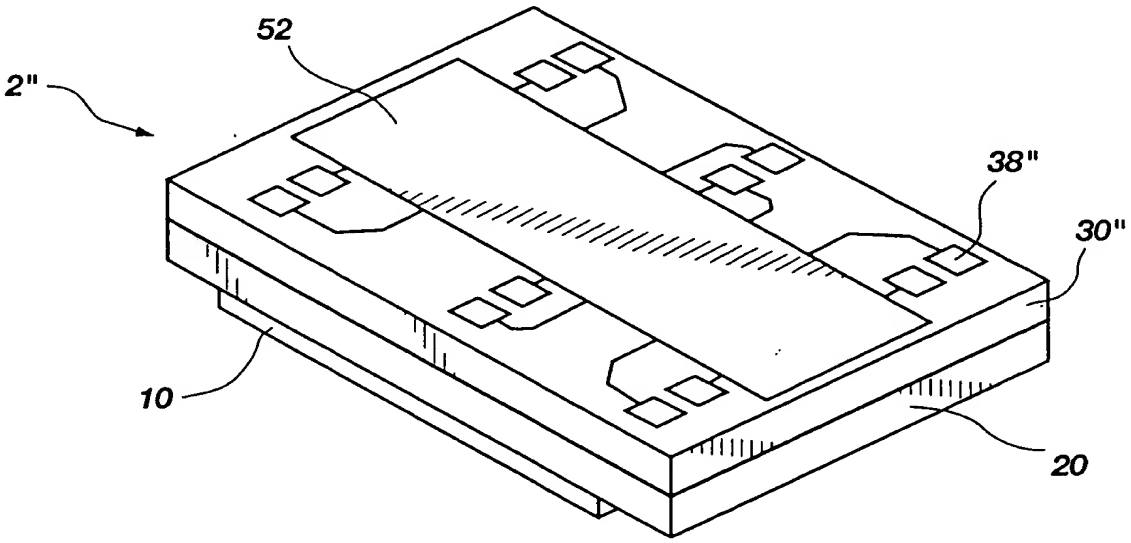


Fig. 7B

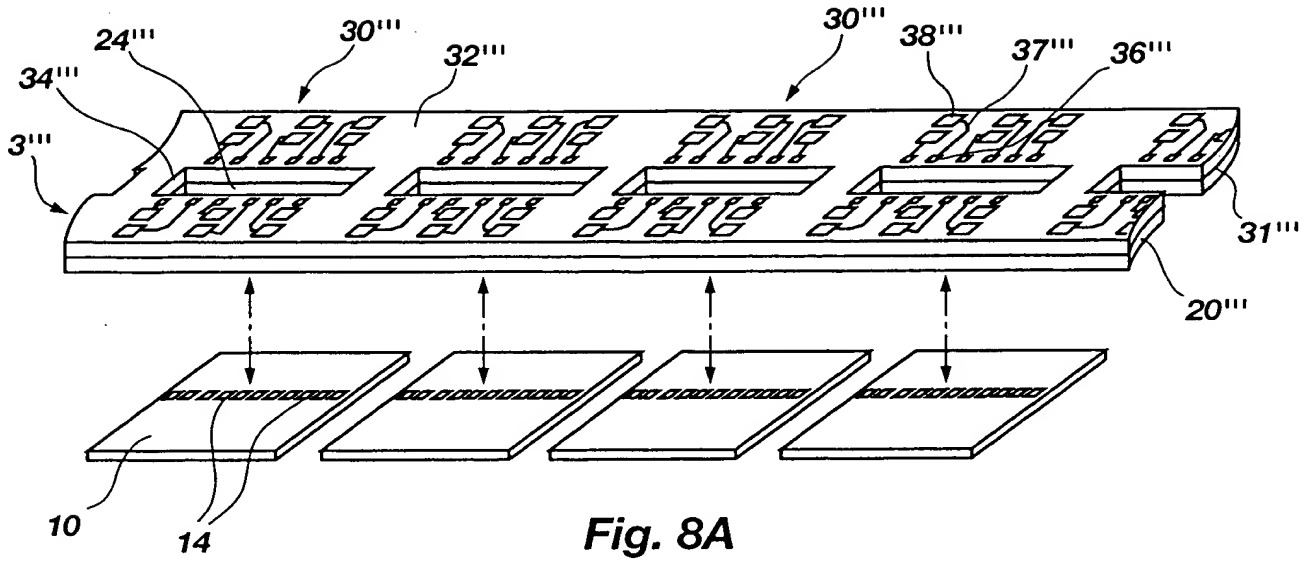


Fig. 8A

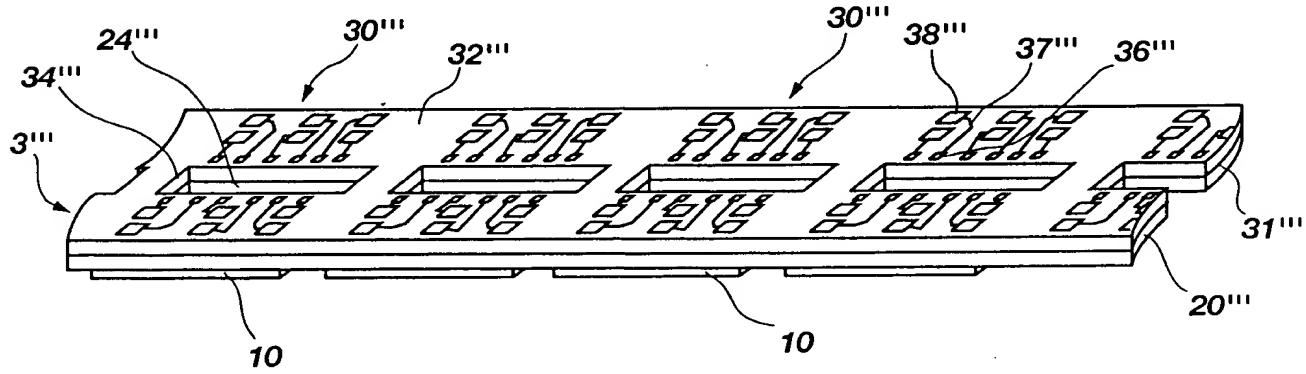


Fig. 8B

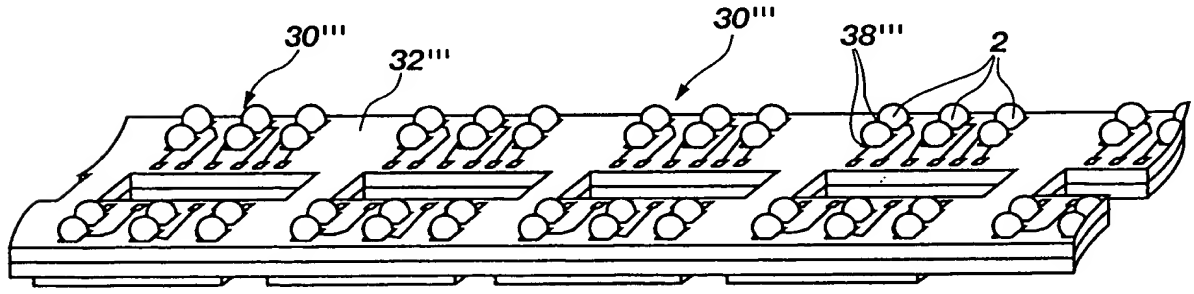


Fig. 8C